REMARKS

In a final office action dated April 19, 2004, the Examiner rejected claims 1-15 under 35 U.S.C. 102(b) as being anticipated by Janik et al. (U.S. Patent 6,163,839).

Applicants have amended independent claims 1, 8 and 15 to more specifically recite significant features of the claimed invention. In particular, the independent claims are amended to recite that the data tags are always in the same pipeline stage as the data with which they are associated. As amended, the claims are patentable over the cited art.

In the previous office action, the Examiner rejected all claims as anticipated by *Janik.* Applicants responded by amending the claims are explained the difference between the claimed invention and *Janik.* The remarks accompanying the amendment are still germane, and are incorporated herein by reference.

As explained in response to the previous office action, applicants' invention relates to stage control in an asynchronous pipeline. Unlike a conventional synchronous pipeline, in which data advances from one stage to the next responsive to a global clock signal, an asynchronous pipeline does not use such a global clock to control advancing through pipeline stages. In an asynchronous pipeline, data advances to the next stage when the pipeline is ready, as determined by internal pipeline logic. The asynchronous pipeline is thus potentially faster, since it doesn't need to wait for the worst case stage delay, but the variable delay makes it more difficult to predict data progress through the pipeline.

In accordance with applicants' invention, a data tag is associated with each data set processed by the pipeline, the tag accompanying the data set through each successive stage of the

pipeline, so that the two are always together. Advancing from one stage to the next is controlled by internal logic which uses, among other factors, a comparison of the data tag with a control tag. The data set and its tag are allowed to advance to the next pipeline stage only if the data tag matches the control tag. Typically, some other condition or conditions, which may be conventional, must be met in addition to matching the data tag with the control tag. Use of the data tag and control tag to control advancing through the pipeline permit external logic to control the asynchronous pipeline, so that, e.g., data sets may be halted at some arbitrary stage pending some other action, timed according to some external timing conditions, etc.

Janik discloses a synchronous "counterflow" pipeline architecture for a processor, in which an instruction pipeline is arranged in physical proximity to a result pipeline, the two flowing in parallel and in opposite directions. Stages in the instruction pipeline correspond to stages in the result pipeline in reverse order, allowing results of recent operations to be transferred to the instruction pipeline where needed in a subsequent operation. When ready to execute, an instruction is dispatched to an execution unit. Results from the execution are placed in the result pipeline in the first available slot. A tag is associated with instructions and results, by which it is possible to match results with the instructions which produced them. This is necessary because results are not always produced in sequence.

The differences between *Janik* and applicants' invention are so numerous that it is hard to know where to begin. But as a fundamental starting point, one must bear in mind that *Janik*'s device is a set of ***synchronous*** pipelines, i.e. pipelines synchronized to some clock signal. Indeed, this is the whole point of *Janik*'s counterflow architecture. As explained at col. 7, lines 12-30, the counterflow architecture is intended to facilitate a fast clock cycle. *Janik*'s invention allows instructions to wrap around to the beginning of the instruction pipeline where required result operands are not yet available in the results pipeline. This feature is necessary because the

pipelines operate on a fast, synchronous clock, and so must be kept moving. Applicants' invention, on the other hand, utilizes an ***asynchronous*** pipeline, in which the data tags which accompany data through the pipeline are used for external control. The whole notion of wrapping, upon which *Janik*'s invention is based, is irrelevant because the data tags always accompany the data.

In attempting to clarify this and other distinctions in response to the previous office action, applicants amended the claims to recite that the data tags and data sets pass through the pipeline "in unison". In their remarks accompanying the amendment, applicants argued that *Janik* was distinguishable because, inter alia, the amended claims recite in essence that the data tag is always in the same pipeline stage as the data with which it is associated.

In the recent office action, the Examiner rejects this distinction on the grounds that it is not set forth in the claims. The Examiner takes the position that the words "in unison" mean only occurring at the same time, and that *Janik*, being a set of synchronous pipelines, necessarily discloses events occurring at the same time.

Applicants believe that the Examiner's reading is erroneous. The Examiner focuses on the single phrase "in unison", while ignoring the rest of the clause of which it is a part. The claims recite that specific things occur in unison, i.e., that "said respective data tag value passes through each successive stage of said plurality of stages of said asynchronous pipeline in unison with said data set to which the respective data tag value is assigned" (claim 1). By reciting that the tag value passes through "successive stages" in unison with the data set, this limitation necessarily means that they are in the same stage together, and accompany each other through successive stages.

Although applicants believe that the Examiner is taking an unreasonably expansive interpretation of the applicable claim limitation, in order to further prosecution herein, applicants have added the further limitation that the tag values are always in the same pipeline stage as the data to which they are assigned or correspond. Applicants believe this limitation is merely redundant, but are willing to make this aspect explicit if the Examiner feels the existing claim language is ambiguous.

Applicants' representative amended claim 1 recites:

> 1. A method for externally managing data within an *asynchronous pipeline*, wherein said asynchronous pipeline includes a plurality of pipeline stages, and a data path and a control path traversing said plurality of pipeline stages in unison, said method comprising:
>
> assigning a respective data tag value to each of a plurality of data sets, each said data set for input to said *asynchronous pipeline* in a respective input interval;
>
> sending each said respective data tag value into said control path when said data set to which the respective data tag value is assigned is sent into said data path such that said respective data tag value passes through each successive stage of said plurality of stages of said asynchronous pipeline in unison with said data set to which the respective data tag value is assigned, *each said respective data tag value always being in the same pipeline stage as the data set to which the respective data tag value is assigned*; and
>
> comparing each said data tag value with a respective control tag value associated with a given stage of said *asynchronous pipeline*; and
>
> in response to a data tag value matching a respective control tag value, permitting said matching data tag value and the data set to which said matching data tag value is assigned to pass in unison to a next stage within said *asynchronous pipeline*. [emphasis added]

Independent claims 8 and 15, although not identical in scope, contain limitations analogous to the italicized language.

Janik does not disclose any "tag" satisfying the recited conditions. The Examiner appears to read the recited "tags" on values in *Janik*'s instruction pipeline. Due to *Janik*'s counterflow architecture, data in the instruction pipeline (alleged "data tag") is not always in the same or corresponding pipeline stage as data in the result pipeline (alleged "data with which it is

associated") as data moves through successive stages of the pipeline, as recited in applicants' independent claims, and accordingly the claim limitations are not met. *Janik* discloses something it calls "tags", but these are used to match data with the instructions which produced them, and not to control the passage of data from one pipeline stage to the next. For all these reasons, as well as those stated in response to the previous office action, the amended claims are not anticipated by *Janik*.

Nor are the amended independent claims obvious over *Janik*. Although *Janik* discloses asynchronous pipelines in its background, and suggests the use of asynchronous pipelines in the general sense, there is no specific disclosure of how the passage of data from one successive pipeline stage to the next would be asynchronously controlled. At most, *Janik* suggests that a pipeline apparatus similar to that disclosed in the patent could be controlled asynchronously using conventional means, as opposed to control by a clock as in the preferred embodiment. As explained, the entire motivation of *Janik*'s counterflow architecture is to improve clock speeds, implying a synchronous mode of operation. There is no teaching or suggestion that tags which accompany data through successive pipeline stages, always being in the same stage as the data to which they correspond, would be used to control the passage of data from one pipeline stage to the next, as recited in applicants' claims. Accordingly, any suggestion to modify the operation of *Janik*'s tags in some way as to come within the scope of the claims is absent, and the claims as amended are not obvious over *Janik*.

In view of the foregoing, applicants submit that the claims are now in condition for allowance and respectfully request reconsideration and allowance of all claims. In addition, the

Examiner is encouraged to contact applicants' attorney by telephone if there are outstanding issues left to be resolved to place this case in condition for allowance.

Respectfully submitted,

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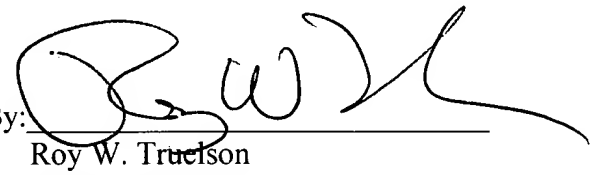
By: 

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